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Synopsys' Great Chip Series

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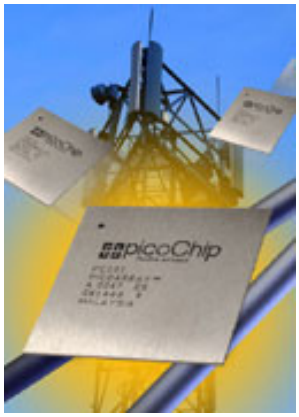

picoChip Designs PC101 picoArray
With computational power of 30 Giga-MACs per second and claimed to be 12 times faster than its nearest competitor–with a modest 160MHz clock rate–the PC101 Software System on a Chip aims at cutting the cost of third-generation mobile infrastructure. By providing a re-programmable base station, it offers the ultimate field flexibility.

"Our architecture brings together 430 powerful processors on one die," said Rupert Baines, vice president of marketing at picoChip. "By defining the communication between the processors at compilation time, the solution is scalable and easily re-programmable."

Believed to be the largest IC design undertaken in Europe, the PC101 has won the award for best-newcomer category and came runner-up for best-design solution category at the prestigious Electronics Industry Design Awards for 2003. The PC101 has also been short-listed for the Design Application award at the forthcoming European Electronics Industry Awards for 2003.

"By focusing on the specific needs of the 3G wireless base station market, we have architected a solution based on a parallel design which doesn't suffer any of the disadvantages of traditional parallel processors," continued Baines. "It's straightforward to program–especially as we ship the product with a complete-tool chain and UMTS systems library–and the communication between processors is optimized for the specific problem we're solving."

Facing Tough Design Challenges
"We faced design challenges at various levels, " said Baines. "Architecturally, we had to balance the processor granularity and speed to get the right throughput for this particular application. To help keep power dissipation at reasonable levels, the clock speed is moderate by today's standards. However, as we're packing a lot of processing into each clock cycle, achieving timing convergence was still a challenge when we came to implement the architecture."

WEB LINKS

- www.picochip.com
- Electronic Design Industry Awards 2003
- European Electronics Industry Awards 2003

"Our architecture brings together 430 powerful processors on one die". -- Rupert Baines, vice president of marketing at picoChip.

“Although the majority of our design flow is based on Synopsys, this is not down to following a ‘single-vendor’ policy,” continued Baines. “We have evaluated each tool on its own merits. Our Verilog-simulation flow is built around VCS™, which provides us with an excellent price-performance point for module verification using desktop PCs, as well as high speed and capacity, complementing our PC/Linux platform solution.”

Key Tools in picoChip’s Design Flow

- Verification – VCS™
- Synthesis – Design Compiler™
- Static Timing Analysis – PrimeTime®

Technical Chip Specifications

- 20-million gates
- Clock-rate 160MHz
- Fully synchronous
- 200 Giga-instructions per second
- 140 Giga-operations per second
- 30 Giga-MAC per second
- I/O bandwidth: 8.9 Gbps
- 0.13-micron, 8-layer copper process
- 430 processors

PicoChip Designs at a Glance

Located in Bath, England picoChip, provides fast, flexible wireless solutions for next-generation telecommunications systems. picoChip offers a 2.5G and 3G (Node B) infrastructure-technology platform to help equipment makers minimize time-to-market, costs, and system-power consumption.

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- ○ Exceptionally informative (I emailed the article to a friend)
- ○ Very informative
- ○ Informative
- ○ Somewhat informative
- ○ Not at all informative

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