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Integrated Circuit Design Facing Maximum Economic Pressures Today

By Mike Harris

Aart de Geus, chairman and chief executive officer of Synopsys, Inc., gave the keynote address entitled "Electronic Design Under Max Pressure" at the annual Synopsys Users' Group (SNUG) meeting held in San Jose, CA, March 17-19.

De Geus spoke about the reasons why integrated circuit design is under maximum economic pressures today, and offered solutions for reducing these pressures going forward.

"There's a lot of pressure on the technical side and on the economic side," said Aart de Geus. "We have to conclude that the pressure is really on every side. Starting with design cost and design complexity, there's absolutely a discontinuity from what we've seen in the past."

De Geus noted that in the past the electronics industry has seen Moore's Law growing unabated. He clearly sees that the costs to build fabs and the costs to develop new silicon technology node points have risen dramatically. The biggest pressure may be the economy. To make his point, de Geus looked at the big picture and zoomed in gradually to the semiconductor domain and then into IC design.

"Starting with the economic pressure, obviously, it's highly visible especially in the last few days [the beginning of the Iraq War] that we have a political situation that is putting quite a bit of pressure on the economics," said de Geus. De Geus said he has spoken with many semiconductor executives, but some were a little "fuzzy" about the political situation, stating that they believed that it is probably costing them about 10 percent of their business. (Figure 1).

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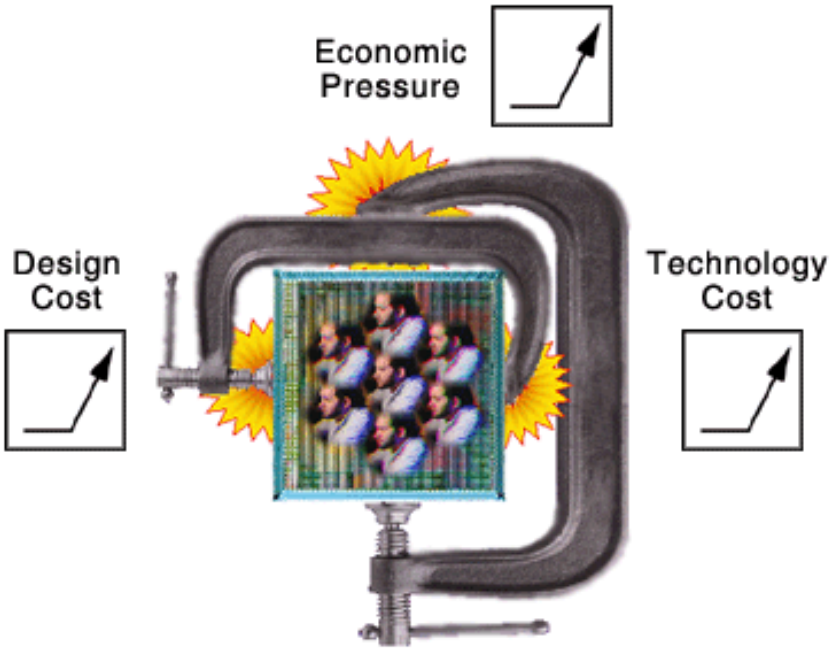

Figure 1. The pressure is mounting

The reality is that these economic pressures are quite painful. Some examples: A practical measure of this can be seen in terms of the price of oil. The price per barrel has increased substantially. Every $10 increase in the price of a barrel of oil costs roughly 0.5% of GDP growth, which has a tremendous impact on the overall economic situation. Overcapacity in the airline industry is also highly visible. This curve may get worse as fewer and fewer people travel for business or pleasure. Another example of overcapacity is the vacancy rates in commercial real estate in Silicon Valley, according to de Geus. “In 1999-2000 way too much was contracted up and then the dot.com bubble burst.”

Pressures Facing the Semiconductor Industry

The semiconductor industry is facing enormous pressures today. “If you look at the content of semiconductor value in terms of products in the last 40 years, the industry has grown dramatically, and the growth has come in waves,” said de Geus.” “The PC was a big wave. The embedded processor, wireless, networking wave was enormous. But there is also a sense that the growth rate cannot continue.”

But there is more growth coming, according to de Geus. “We will keep seeing growth, but it will be more moderated than what we’ve seen in the last 20 years.” Moore’s Law will make it possible to invent new products. However, price will have the greatest impact on the semiconductor economy. Price is usually dictated by supply and demand. Looking at the utilization of the chip fabrication plants that are in place, one can clearly see that there’s a big differential between supply and demand. Today, there are more fab lines, specifically 300-millimeter lines, coming online. According to de Geus, a big increase in price in the next three quarters is not predicted.

The semiconductor industry has gone up and down over the last 20 years because there's a continual misalignment between supply and demand. As soon as there is high demand, people start adding supply. It takes about 18 months and when the supply comes online, over-supply occurs.

Until recently, 1985 was the worst downturn in the history of semiconductors. After about 15 months, it turned back up sharply. Today, the industry is in the upswing of one of those waves again. The depth of past waves has been about 26-27 percent from its peak. The curve that semiconductors are riding right now is about twice as bad as seen before in the history of semiconductors. It was down about 40 to 46 percent in 2001 and down about 33 percent in 2002. (Figure 2).

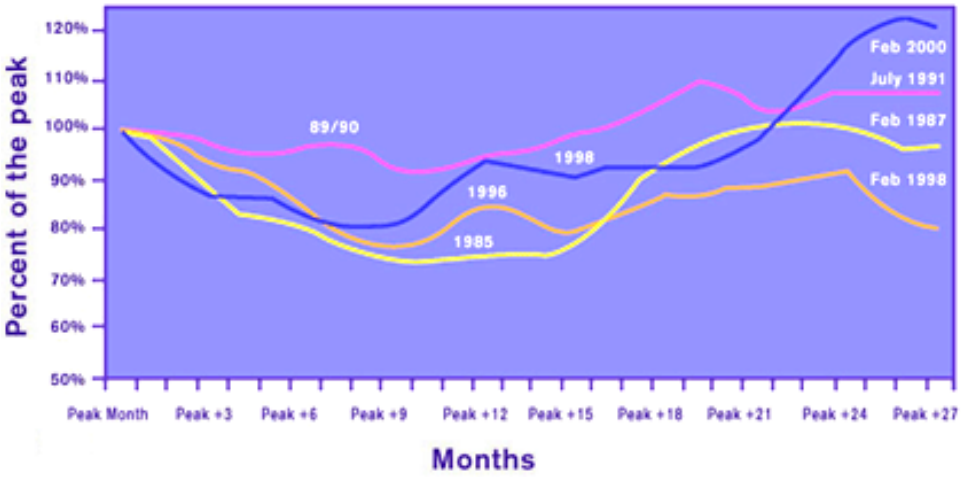

Figure 2. Semiconductor sales downturn

Overall, de Geus believes that the semiconductor business will see a gradual return this year and in 2004 as well.

Pressures Continue for Semiconductor Providers; Challenges Greater

What makes the challenge greater today for semiconductor providers? The cost of silicon technology has gone up significantly. Cost includes the economics of risk management. Advanced chips are being designed at 130 nanometer as the industry transitions to smaller and smaller geometries. Most chip fabrication is at 180 and 250 nm, or at 0.25 micron. "There are a few advanced designs–and we know of roughly 50–that are being created with Synopsys' tools at 90 nanometer," said de Geus. " These are the most advanced, practically prototypes, but not necessarily production designs."

The transition to 130 nanometer was not smooth because there were significant yield issues. Not only are the lithography techniques very sophisticated, but also the industry has now gone to a new set of materials. Specifically, low-k dielectrics have brought about a number of surprises. Another important aspect is that the cost of putting in a new node point is substantial–about $500 million to $1 billion. In addition, to put in a 300mm fab costs

approximately $2.5 billion, so not many companies can actually afford this.

Mask making takes place before the actual fabrication. While the cost of masks is roughly related to the number of rectangles that make up the mask, a mask-set can now cost $500,000 to $700,000. “The number of companies that can actually play and put in place a complete fab is diminishing,” noted de Geus. “This is what we call the ‘billion dollar club,’ he added, ” and the number of companies that year after year have put in a billion dollars in investment is decreasing. The next set of pressure points is technology cost.”

A Walk on the IC Design Side

There are substantial challenges and pressures on the IC design side. Chip designers’ skills will be taxed even more. Starting with the basic news that Moore’s Law is alive and well and expected to continue for the next decade, the number of transistors will continue to increase. “This opens up opportunities for new products,” said de Geus. “Whenever you get another 10X of capabilities on a chip, it makes it possible for the creation of exciting new products.”

According to de Geus, innovation is alive and well in the electronics environment. As designers go to smaller geometries, the number of designs that actually meet specification is decreasing. Moreover, the number of designs that are operating as expected–at the speed and power consumption that one would like–is also decreasing. A side effect is that the number of full mask re-spins is increasing.

Design Point of View: Implementation and Verification

There are things that need to be mastered both from an implementation point of view and from a verification point of view. Starting with implementation, complexity of chips is driving both the “opportunity space” and the challenges. And with that comes not only hierarchy, but also the need to work at both the top level and at the detail level to make everything work together. “By ‘together’ we mean that the singular thing that designers will keep driving going forward is timing—the speed of the chips,” said de Geus. “And timing closure, in my opinion, will remain the toughest, but also most exciting, challenge in IC design.”

Timing closure got a littler harder because signal integrity is starting to move designers another step away from traditional digital design. Today, designers must deal with the fact that because the sheer geometry size is so small–a physical phenomenon that before could be overlooked–timing-closure becomes an increasing significant part of the design flow.

Chip Verification Has Its Own Brand of Pressures

On the verification side, pressures exist, too. First, verification descriptions are growing dramatically, more rapidly than Moore’s Law. Second, there is a need to verify not only the logic and the

analog portion, but also the complete system in an integrated fashion. In other words, mixed-signal representations and manipulations will increase. Third, the actual simulation cost and number of simulation cycles are increasing dramatically. “The good news is that we have definitely been able to take advantage of Linux farms, low-cost, high-performance processors that increasingly are being used in large arrays,” noted de Geus.

The result is that today verification takes anywhere between 60 and 70 percent of overall design time. In chip verification there have been a number of waves and pressures over the years, starting with SPICE as the transistor-level simulator of choice, then gate-level simulation and RTL. What’s next? About 15 years ago there were a lot of languages and a lot of formats, all working together. However, a design gap emerged, and the breakthrough was the introduction of RTL languages and hardware description languages. This was a big breakthrough, because a lot of designers could shift from thinking in schematics to thinking in languages. The downside to this breakthrough was that there were two languages, instead of one.

Today, the VHDL and Verilog languages have made it possible to design complex chips, with a big boost specifically in the early ‘90s. For the last three or four years, IC designers have become very worried about the amount of time that verification is taking. This worry and pressure has fostered innovation. New techniques are developing: efforts in formal verification, in testbenches, in coverage metrics, in mixed languages, in system languages, and so forth. “Synopsys is at the beginning of a massive rallying point in all these topics,” said de Geus. “I believe that the opportunity for success will be influenced significantly by System Verilog. Moreover, at Synopsys we’re putting significant weight behind this language for RTL-plus design.” (Figure 3).

Figure 3. System Verilog: Next-generation Verilog

Synopsys believes there is a whole realm of design that is oriented towards the C language, because a good deal of embedded software is there at the transaction level. “At the RTL-plus level, though, SystemVerilog will be the major replacement, and the objective will be to make this transition as smooth and painless as possible,” said de Geus.

What about VHDL? SystemVerilog takes much from the Verilog language, although it has learned a number of lessons from VHDL. “Synopsys’ objective will be to make sure that over a number of years, we will provide a mixed-language environment so that none of a designer’s VHDL work is lost,” said de Geus.

SystemVerilog is not only a language; it’s also opening a new age. After 15 years of simulation, designers are now going to take the simulation techniques, formal verification techniques, test tracing techniques, and synthesis techniques, and put those together in the design-for-verification age.

System Verilog Asserts Assertions

“Starting the second half of this year, we’re opening the new era of design for verification. In this realm, assertions on a design are absolutely key,” said de Geus. “ If there are assertions inside the same description code that’s being used for implementation and verification, you can spawn off from there a variety of tools, be they formal tools, simulation tools, coverage tools, and so forth–all from the same source code.” (Figure 4).

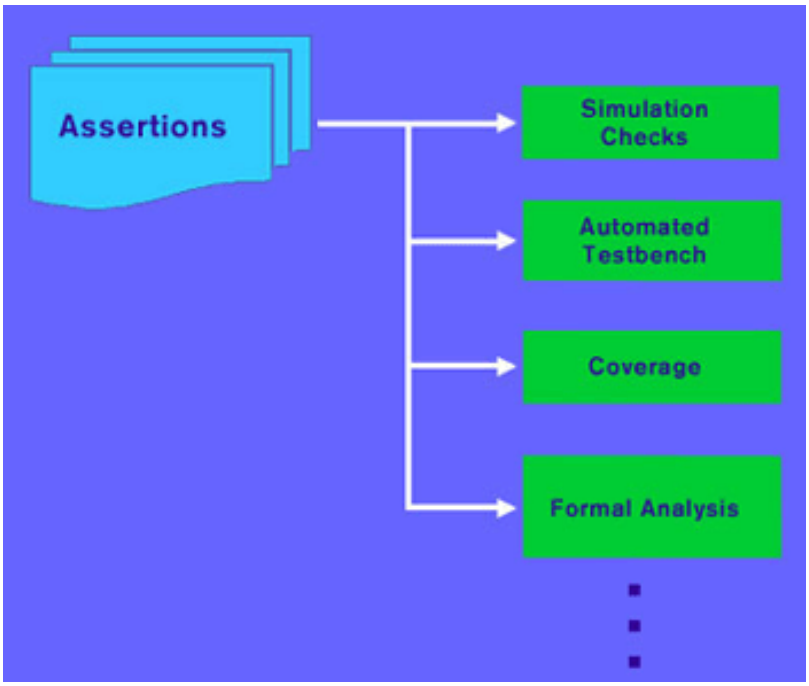

Figure 4. System Verilog provides assertions for a single point of specification

What are “assertions”? Essentially, they are temporal statements. An example would be one that says that a certain signal will occur only in a certain window after another signal. The key to assertions is that they should be implemented during the design. IC designers want to capture the knowledge that they have of their design in a broader fashion, including many of these assertions and constraints. “If we look at a designer of the future, he or she will capture a number of these assertions and then apply them automatically to the overall system,” said de Geus.

Where is the field going? “We’re going to see the big benefits in a

combination of formal techniques and simulation techniques that are directed by the assertions and the constraints," said de Geus.

Reducing Pressure from Maximum to Minimum
In the last 30 years, the industry has learned to live up to the growth in silicon opportunities. Again, Moore's Law is at work, but the silicon opportunity keeps growing. The IC design community continually revamps by designing with new tools, new methodologies and with new levels of abstraction. Innovation quickly translates into application

Timing Closure Less of a Pressure Problem
Timing closure became a big problem during the last four or five years. Physical synthesis was the first step to address this problem. "I'm convinced that timing closure will remain the key to tying together different tools and will be the real metric of success for a good design flow," said de Geus.

Milkway Database Also Helps Reduce Design Pressures
Synopsys has opened up the Milkyway database and its interfaces so that designers can connect either competitors' tools or internal tools to it. Because Milkyway has already been used on thousands of the most advanced designs, has rapidly become the *de facto* standard.

Power as a Problem in Chip Design
Power is becoming a bigger problem. "I heard an interesting story from the CEO of Google," recalled de Geus. "He said, 'You know, if I look at my computer farm right now, the cost of power and power dissipation for one year in California is greater than buying a single computer."

Cost of Test Is Yet Another Pressure
Test is yet another area that has experienced a rapid increase in cost in the last few years. But Synopsys offers some good news in this arena. "We take the tester and put some of that functionality on the chip," said de Geus. "Essentially, the chip tests itself." According to de Geus, this is a technique that's not new, but has been used for memories for a long time, although never really that effective for logic. Last fall, Synopsys announced its first chip back from fabrication that clearly demonstrated great savings in the number of tests that the tester had to execute on the chip, directly impacting the cost.

Intellectual Property
Verification intellectual property (IP) will be a bigger task ultimately than implementation IP. For that reason, Synopsys has invested substantially in the last two years in those IP blocks. Synopsys has an increasingly large collection of recognized models. They have also invested in the standard IP that connects things on a chip. Today, Synopsys provides the IP to create all of this from scratch, fully synthesizable and optimized for speed and area.

Intellectual property is now being reused more and more by Synopsys and a broad set of other companies. “I do think that design for verification is a set of techniques that will keep improving things,” said de Geus. “I believe that really good IP will be difficult to build. It’s not just the implementation; it’s optimization for different technologies, verification sets, test sets, and so forth, but Synopsys provides most of this.”

Pressures will Decrease and Design Challenges will be Overcome

Although economic pressures surrounding integrated circuit design most likely will continue for the near term, IC designers facing problems are finding solutions everyday. “I think it’s fair to say that times are pretty tough, and the squeeze is on,” said de Geus. “However, I am a strong believer that when times are tough, the most competent people ultimately win.”

Mike Harris is editor in chief of Compiler Magazine. Formerly, he was editor in chief of Electronics Journal, published by Avant! Corporation. (Avant! was acquired by Synopsys in June 2002).

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